AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Original) A flash memory cell, comprising:

a tunnel oxide film formed at a given region of a SOI substrate;

a floating gate on the tunnel oxide film;

a dielectric film on the floating gate;

first and second channel regions at the SOI substrate below both ends of the floating gate;

a source region formed between the first and second channel regions;

first and second drain regions at the SOI substrate at both sides of the floating gate; and

a word line formed on the dielectric film,

wherein data of two bits or four bits are stored at a single cell by individually injecting electrons into the floating gate on the first and second channel regions or discharging the injected electrons, depending on voltages applied to the source region, the word line, and the first and second drain regions.

2. (Original) The flash memory cell as Claimed in claim 1, wherein said floating gate is consisting of a nitride film.

3. (Original) The flash memory cell as Claimed in claim 1, wherein the first and second channel regions each consist of a P type impurity region and wherein the first and second drain regions consist of a N type impurity region.

4. (Original) The flash memory cell as Claimed in claim 3, wherein the first and second drain regions are formed in a P type impurity region forming the first channel region and a P type impurity region forming the second channel region, respectively.

5. (Original) The flash memory cell as Claimed in claim 1, wherein a lower portion of the source region is precluded from an insulating film included in the SOI substrate, by which the source region is electrically isolated from other source regions.

6. (Original) The flash memory cell as Claimed in claim 1, further comprising a device isolation film formed on the first and second drain regions, wherein the floating gate is separated by the device isolation film.

7. (Original) The flash memory cell as Claimed in claim 1, further comprising a contact plug formed to be electrically connected with the source region, and the first and second drain regions.

8. (Original) The flash memory cell as Claimed in claim 7, wherein said contact plug is included one by one every 5 through 10 cells and the number of the contact plug is controlled by a design rule or a voltage to be applied.

Claims 9-40 (Canceled)